# ECE 385

Spring 2022

Experiment #1

# Lab 1

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**Thursday 8a.m.-11a.m. D225**

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**Purpose of Circuit**

The primary purpose of the Lab 1 circuit is to design a 2-to-1 multiplexer with 2-input NAND gate chips. Furthermore, we redesign the circuit to solve the “glitches” problem which is caused by the properties of logic gate itself, and the performance of the circuit is improved after that.

**Written Description of Circuit**

The circuit is designed based on the concept of 2-to-1 multiplexer, which is supposed to have the following K-map.

形状

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Figure . K-map of the circuit

After correctly circling in the K-map, we can come up with the logic expression: Q = AB + B’C, and the circuit design with 2 AND gate and 1 OR gate to accomplish the multiplexer. However, under the preference of using NAND gate only instead of AND and OR, we shall use de Morgan’s Law to further adjust the expression to: Q = ((AB)'(B'C)')'. Notice that we need a converter for B’, but this function can be achieved by connecting both pins of NAND gate with B’s input. Thus, only 4 NAND gates are needed for the circuit design, and we shall have the logical diagram and layout as below.

图表, 散点图

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Figure . Logic Diagram for Multiplexer

图示, 示意图

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Figure . Circuit component layout (blue output)

However, even it’s subtle, we will meet static hazard due to the nonzero propagation delay from NAND gate’s input to output. As a result, in a very short period, the output of circuit is incorrect. It’s more obvious under oscilloscope. In current circuit, both A and C provides high-voltage (1) input, and we will expect the result stays high (1) no matter B’s on or off. But when we switch B to low-voltage (0) input, there is a gap appear in the output, indicating a temporary wrong output (0). The fixing process will be shown in the Prelab question B.

图形用户界面

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Figure . Waveform of circuit that contains a short period of wrong output

**Prelab Questions**

Note: Some logic diagram and layout sheet are shown in previous sections.

* 1. Why not all groups may observe static hazards?
     1. Because the static hazard happens in a pretty short period, and the period of it also depends on the specific property (delay and glitch) of the chip we use.
  2. Why does the hazard appear when you do this?
     1. Because it cause a longer delay time to signify the hazard. We utilize a capacitor which cause a short period of time to charge. We count this into the hazard in our lab.

1. Redesign the circuit of part A to eliminate all static-1 hazards (glitches) at the output.

To fix the problem, we look back to the K-map again, and circle an additional term:

图示

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Figure . K-map of the circuit with additional AC term

Now the logic expression from the K-map is: Q = AB + B’C + AC, and if we further change it to adapt the NAND-only circuit with de Morgan’s Law, we will have: Z=((((AB)'(B'C)')')’ (AC)’)’. The advantage to do so is to overlap more logic gates in the circuit to reduce the period of static hazard. The newly optimized logic diagram and circuit layout are in Figure 5 and 6:

图示

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Figure . Logic Diagram for Multiplexer (optimized with AC) 图示, 示意图

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Figure . Circuit component layout (green output)

If we observe the oscilloscope now, the static hazard problem is reduced. Even though there are certain level of noise indicating the switch of B’s input, the overall output stays in the same level.

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Figure . Waveform of circuit that is correct by AC

**Lab Questions**

1. Unit Test
   1. Test has been done, and all gate within the chip works normally.
2. Test part A circuit and complete truth table.

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | Q |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |

Figure . Truth table of part A circuit